FIG. 1
BACKGROUND ART

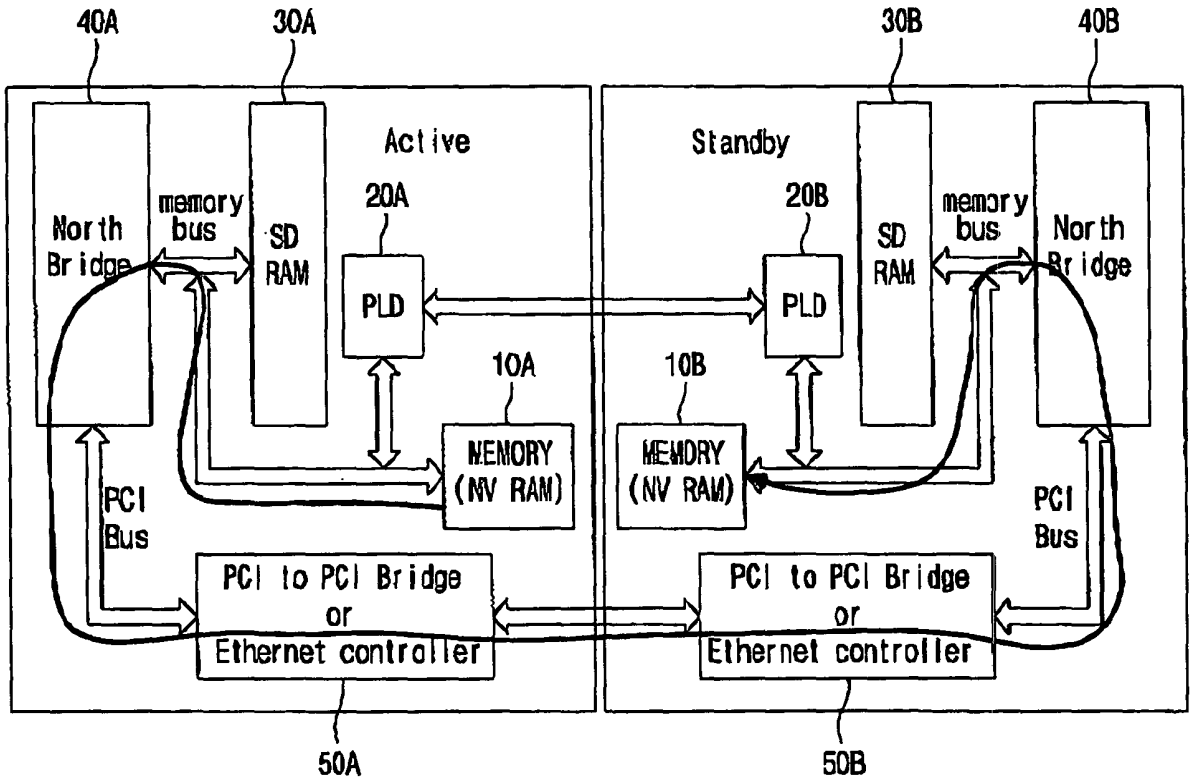


FIG. 2

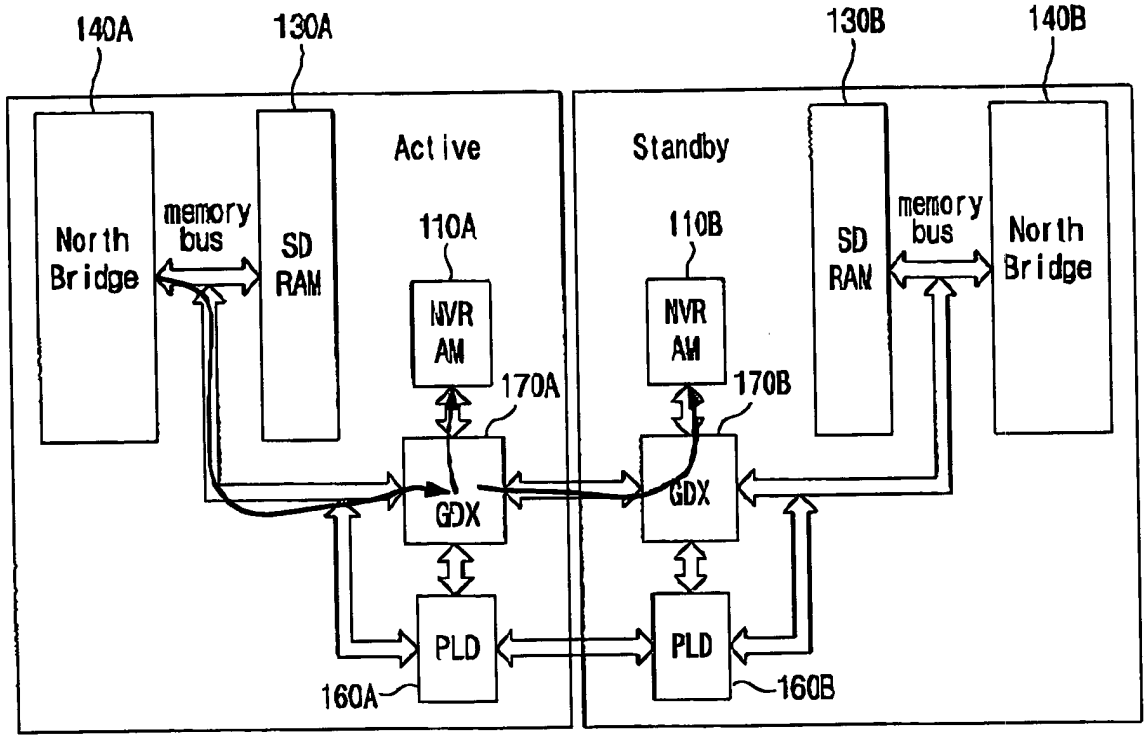

140A
130A
130B
140B
North Bridge
memory bus
SD RAM
Active
Standby
110A
110B
NVR AM
170A
170B
GDX
PLD
160A
160B

FIG. 3

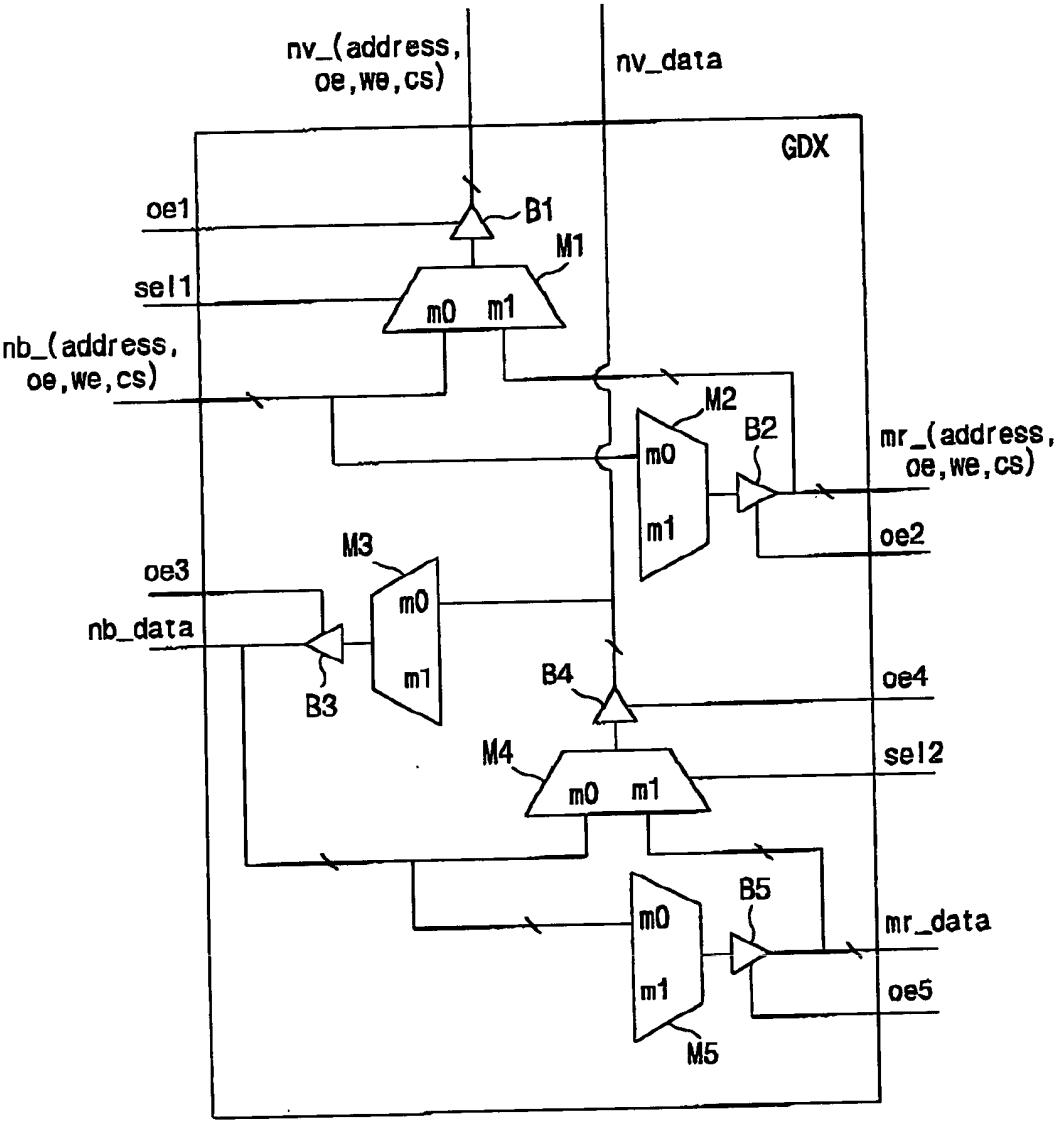

nv_(address, oe,we,cs)
nv_data
GDX
oe1
B1
M1
sel1
m0 m1
nb_(address, oe,we,cs)
M2
B2
m0
m1
mr_(address, oe,we,cs)
oe2
M3
oe3
m0
nb_data
m1
B3
B4
oe4
M4
sel2
m0 m1
B5
m0
mr_data
m1
oe5
M5

FIG. 4

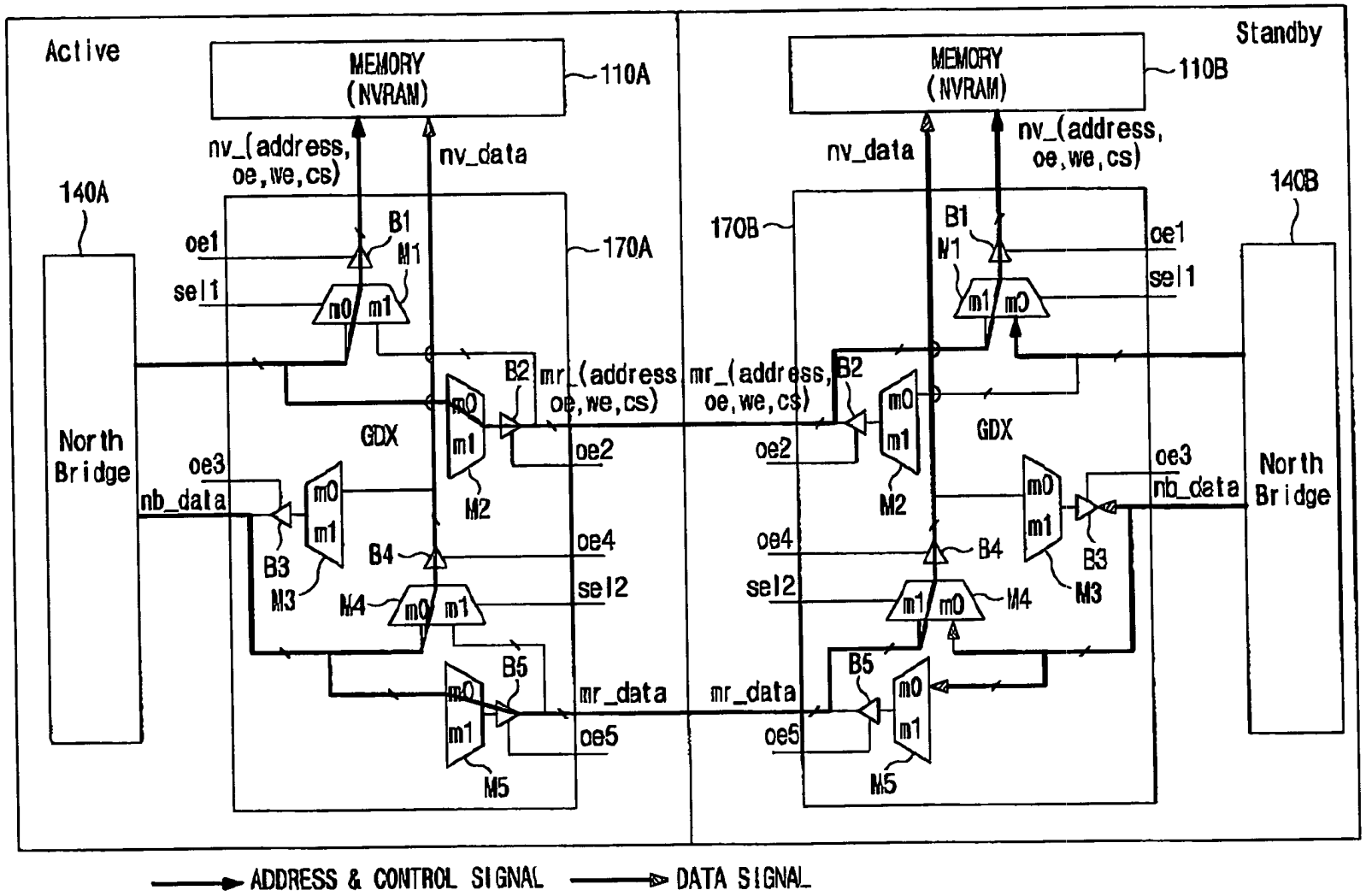
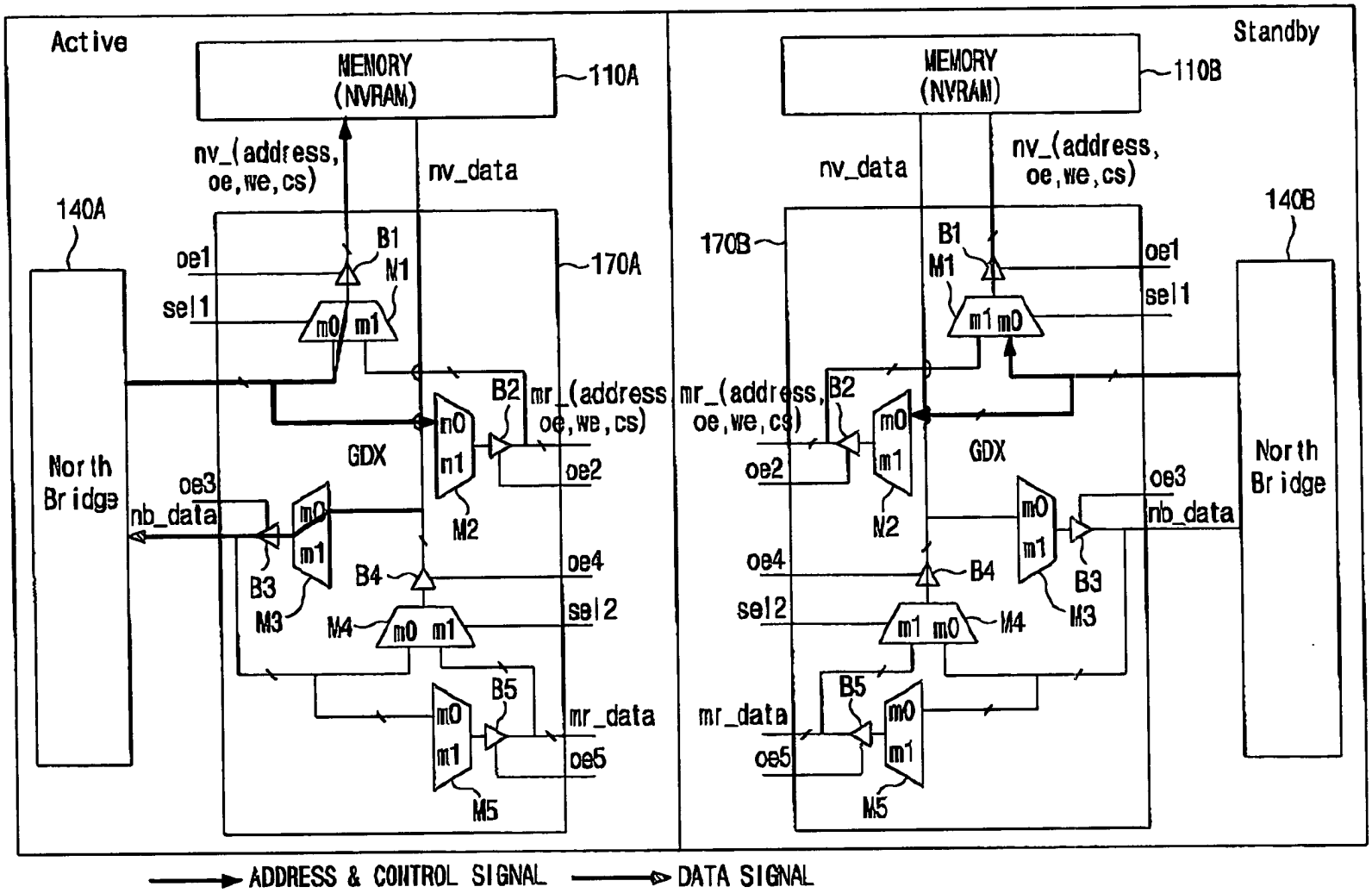

Active
Standby
MEMORY (NVRAM)
110A
MEMORY (NVRAM)
110B
nv_(address, oe,we,cs)
nv_data
nv_data
nv_(address, oe,we,cs)
140A
140B
170A
170B
oe1
sel1
B1
M1
m0
m1
mr_(address oe,we,cs)
mr_(address, oe,we,cs)
B2
M2
GDX
oe2
oe3
nb_data
B3
M3
B4
M4
oe4
sel2
B5
M5
mr_data
oe5
North Bridge
North Bridge
ADDRESS & CONTROL SIGNAL
DATA SIGNAL

FIG. 5



ADDRESS & CONTROL SIGNAL

DATA SIGNAL